# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**Expedited Procedure Requested
Response Under 37 CFR § 1.116**

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| Applicants: | Hiroki KANAI  et al. |
| Serial No.: | 10/025,743 |
| Filed: | December 26, 2001 |
| For: | INFORMATION PROCESSING SYSTEM |
| Art Unit: | 2187 |
| Examiner: | Kimberly N. Mayo |

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**Technology Center 2100**

## AMENDMENT AFTER FINAL REJECTION UNDER 37 C.F.R. §1.116

Assistant Commissioner for Patents                    December 30, 2002
Washington, D.C.  20231

Sir:

In response to the final Office Action dated September 13, 2002, please

amend the above-identified application as follows:

## IN THE CLAIMS

Please amend claims 21, 22 and 29 as follows:

21.  (Amended)  An information processing system according to claim 18,

wherein said memory stores instruction code to be executed on said

processor therein, and said control circuit prefetches the instruction code from

the memory along the first memory bus to said buffer.